CLAIMS

1. A semiconductor memory device comprising a plurality of nonvolatile memories and a controller which controls read/write operations for said plurality of nonvolatile memories through a first memory bus and a second memory bus in accordance with read/write commands from a host apparatus, wherein

when a case where a nonvolatile memory F0 is connected to said first memory bus and a nonvolatile memory F1 is connected to said second memory bus is referred to as a two-memory configuration and a case where two nonvolatile memories F0, F2 are connected to said first memory bus and two nonvolatile memories F1, F3 are connected to said second memory bus is referred to as a four-memory configuration,

said controller comprises:

a selection section which selects one of said two-memory configuration and said four-memory configuration;

a sequential number conversion section which divides each nonvolatile memory into two regions to form a first half region and last half region, and converts a consecutive logical address specified by said host apparatus to a logic sequential number of a predetermined size;

a modulo number generation section which generates a logic sequential modulo number of system of residues of 4 with respect to said logic sequential number; and

a write control section which performs a write operation in a format that selectively and repeatedly circulates through the nonvolatile memories F0, F1, F2, F3 in case of said four-memory configuration and performs the write operation in a format that selectively and repeatedly circulates through the first half region of F0, the first half region of F1, the last half region F0, and the last half region F1 in case of said two-memory configuration based on said sequential modulo number when the write command to the consecutive logical address is made from said host apparatus.

2. The semiconductor memory device according to claim 1, wherein said nonvolatile memory is divided into at least two logical address ranges, and a logical-physical address conversion table is further included for converting the logical address to a physical address for every logical address range.

3. A controller for controlling read/write operation for a plurality of nonvolatile memories through a first memory bus and a second memory bus in accordance with a read/write command from a host apparatus, wherein,

when a case where a nonvolatile memory F0 is connected to said first memory bus and a nonvolatile memory F1 is connected to said second memory bus is referred to as a two-memory

configuration and a case where two nonvolatile memories F0, F2 are connected to said first memory bus and two nonvolatile memories F1, F3 are connected to said second memory bus is referred to as a four-memory configuration,

said controller comprises:

a selection section which selects one of said two-memory configuration and said four-memory configuration;

a sequential number conversion section which divides each nonvolatile memory into two regions to form a first half region and last half region, and converts a consecutive logical address specified by said host apparatus to a logic sequential number of a predetermined size;

a modulo number generation section which generates a logic sequential modulo number of system of residues of 4 with respect to said logic sequential number; and

a write control section which performs a write operation in a format that selectively and repeatedly circulates through the nonvolatile memories F0, F1, F2, F3 in case of said four-memory configuration and performs the write operation in a format that selectively and repeatedly circulates through the first half region of F0, the first half region of F1, the last half region F0, and the last half region F1 in case of said two-memory configuration based on said sequential modulo number when the write command to the consecutive logical address is made from said host apparatus.

4. A method of controlling a semiconductor memory which controls read/write operations for a plurality of nonvolatile memories through a first memory bus and/or a second memory bus in accordance with a read/write command from a host apparatus, wherein

when a case where a nonvolatile memory F0 is connected to said first memory bus and a nonvolatile memory F1 is connected to said second memory bus is referred to as a two-memory configuration and a case where two nonvolatile memories F0, F2 are connected to said first memory bus and two nonvolatile memories F1, F3 are connected to said second memory bus is referred to as a four-memory configuration,

the method comprises the steps of:

selecting one of said two-memory configuration and said four-memory configuration;

dividing each nonvolatile memory into two regions to form a first half region and last half region, and converting a consecutive logical address specified by said host apparatus to a logic sequential number of a predetermined size;

generating a logic sequential modulo number of system of residues of 4 with respect to said logic sequential number; and

performing a write operation in a format that selectively and repeatedly circulates through the nonvolatile memories F0,

F1, F2, F3 in case of said four-memory configuration and performing the write operation in a format that selectively and repeatedly circulates through the first half region of F0, the first half region of F1, the last half region F0, and the last half region F1 in case of said two-memory configuration based on said sequential modulo number when the write command to the consecutive logical address is made from said host apparatus.